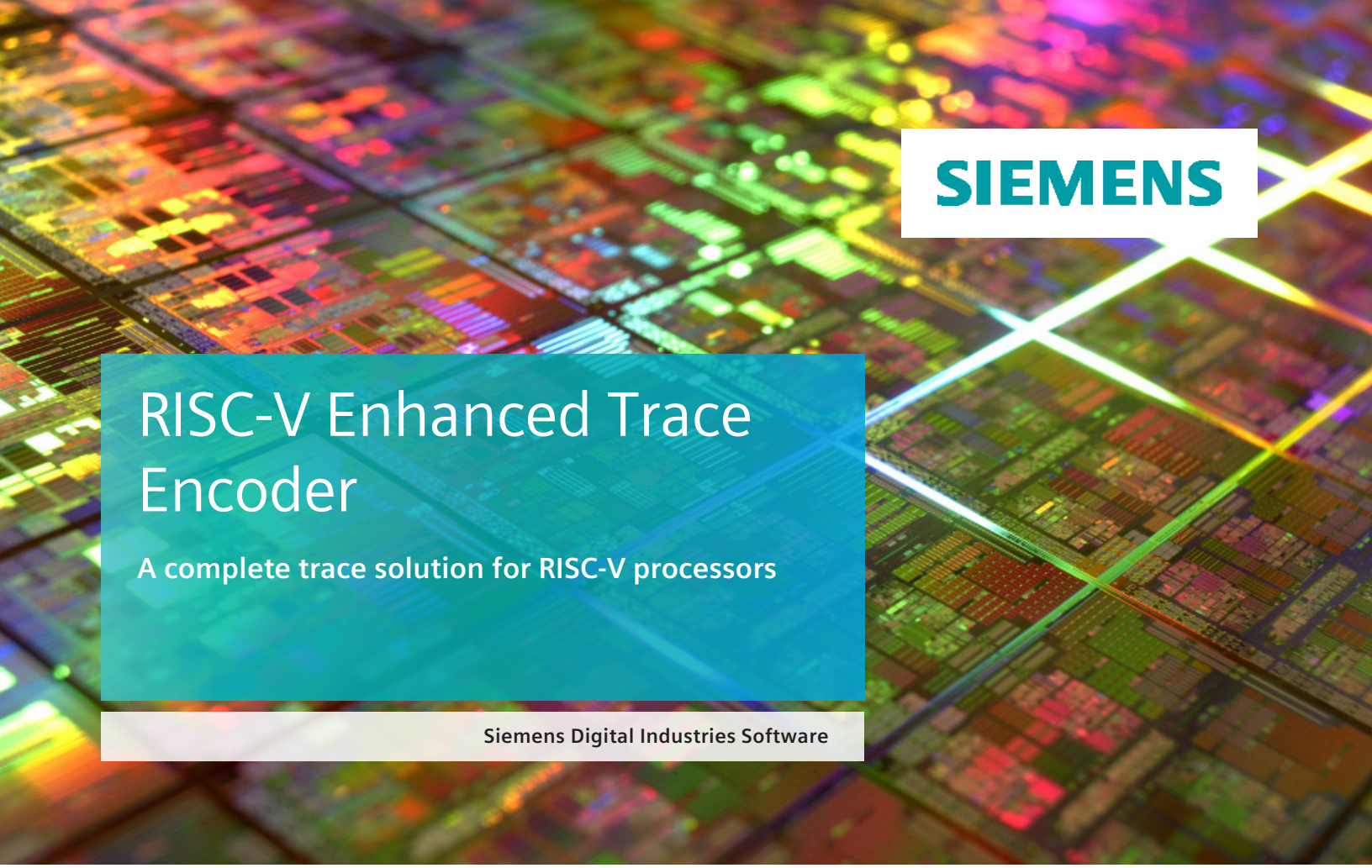


SIEMENS

RISC-V Enhanced Trace Encoder

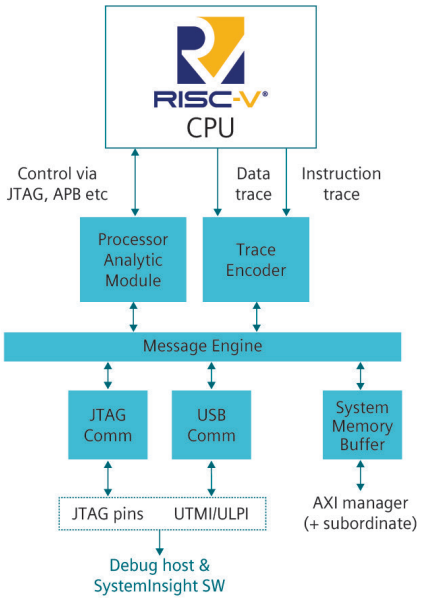
A complete trace solution for RISC-V processors

Siemens Digital Industries Software

At-a-glance

- Generates efficiently encoded instruction and data trace
- Comparators and filters:
  - What to trace
  - When to trace
- Trace buffer
- Message interface
- RISC-V standards-compliant
- Supports 32- and 64-bit CPUs

The Tessent™ Enhanced Trace Encoder is a fully-featured RISC-V trace solution that provides a mechanism to monitor the program execution of a CPU in real time. It encodes program execution (instruction trace) and optionally, the data from load and store instructions (data trace), outputting trace in a highly compressed format. External software can later take this data and use it to reconstruct the program execution flow. The Trace Encoder can be finely tuned to balance the features and gate-count requirements of your system.



The Trace Encoder includes a broad range of filters, giving complete control over what and when to trace. Examples include filters to enable tracing:

- Within an address range
- At a specified privilege level
- Of interrupt service routines
- For a fixed period of time
- Starting and stopping on external events
- ... and many others

The Enhanced Trace Encoder complies with the latest standards produced by the RISC-V International's Efficient Trace for RISC-V (E-Trace) Working Group, supporting any standards-compliant RISC-V processor.

Overview

Complex systems are prone to imperfect software behaviors. These imperfections may be due to several factors, for example, interactions with other processor cores or peripherals, tight timing budgets, poor implementation, or a combination of the above. The imperfections impact the real-time behavior of the system. Software that is not designed to minimize these imperfections leads to avoidable costs, attributed to underutilized CPUs, heating, power consumption, post-deployment defects, crashes, and poor longevity of the systems.

Understanding software behavior can be challenging but is key to tackling the imperfections. Therefore, providing software developers visibility of program execution is vital. Processor trace capability enables the software engineer to view the behavior of a program in detail, instruction-by-instruction without disrupting the system.

However, for maximum effectiveness this needs to be done without overloading developers with vast amounts of data. Enhanced Trace Encoder is designed to ensure that software developers using RISC-V cores can access insights required to optimize their code.

The Enhanced Trace Encoder supports all RISC-V cores with standard-compliant trace interfaces, both 32- and 64-bit designs. Siemens plays an active role in the standard-setting process within the RISC-V International Trace Working Group and supports all standard features in the Enhanced Trace Encoder.

The IP block integrates smoothly with the rest of the Embedded Analytics portfolio, supporting open and industry standard architectures.

Functionality

The Efficient Trace for RISC-V specification specifies a minimum level of trace functionality. The Enhanced Trace Encoder satisfies the full requirements of the Efficient Trace specification, while including many additional features not typically found within implementations provided by CPU vendors or in the open-source community. The following list of features are few of the many features offered by the Enhanced Trace Encoder.

Feature	RISC-V specification	Enhanced Trace Encoder
Instruction trace	Y	Y
Efficient packet format	Y	Y
Fast profiling	Optional	Y
Multiple retirement	Optional	Y
Data trace	Optional	Y
Filters and comparators	Optional	Y
Timestamps	Optional	Y
Implicit return mode	Optional	Y
Branch prediction	Optional	Y
Jump target cache mode	Optional	Y
Implicit exception mode	Optional	Y
Sequentially inferable jump mode	Optional	Y
Cycle accurate trace		Y

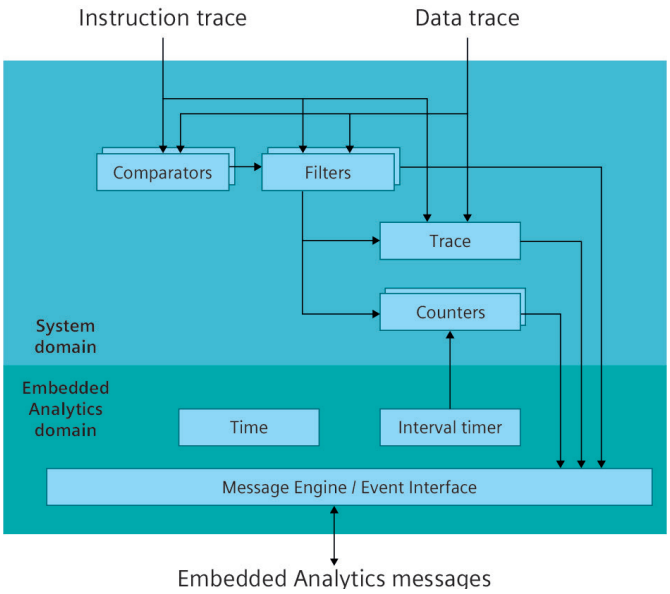
Compliant with Efficient Trace Specification

Instruction trace

- Provides instruction execution information to user
- Most efficient instruction trace within the RISC-V ecosystem
- Enables more and faster trace for same bandwidth and memory

Efficient Packet Format

- The packet format is as per the RISC-V specification



Optional under Efficient Trace Specification

Fast profiling mode

- A non-intrusive alternative to traditional methods.
- When enabled, only reports the address of the instruction immediately following an exception, call or return. Used mainly for code profiling.

Multiple retirement

- Can trace the execution of multiple concurrent instructions from multi-issue CPUs, even when issued out-of-order.

Data trace

- Address and data can be encoded differentially.
- Traces loads and stores to memory that are also traced by the instruction trace decoder.

Filters and comparators
- Reduce the memory and bandwidth requirements for the trace
- Further increase the efficiency of the instruction and data trace

Timestamps
- Provide a method to do very basic profiling

Implicit return mode, branch prediction, Jump target cache mode, Implicit exception mode, sequentially inferable jump mode
- Reduce the memory and bandwidth requirements for the trace
- Further increase the efficiency of the instruction and data trace

Above and beyond the Efficient Trace Specification

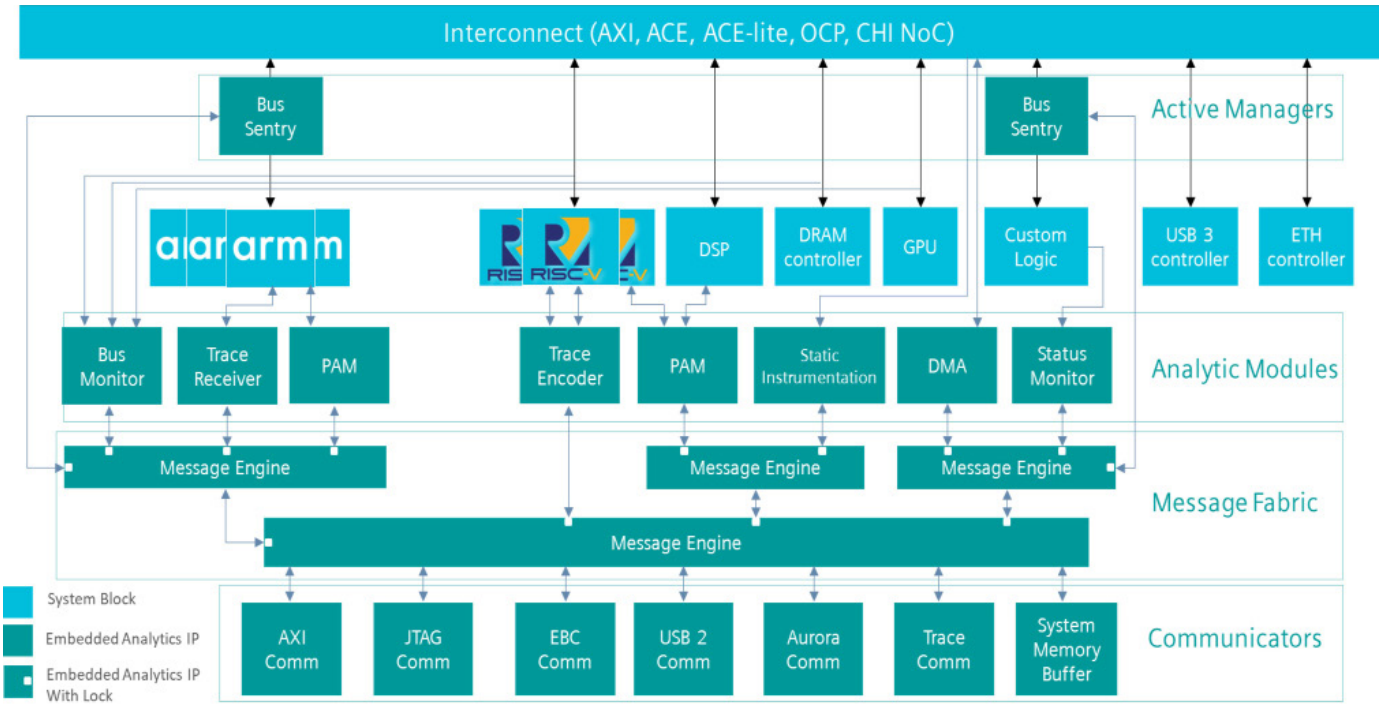
Cycle accurate trace
- Provides timing information that allows the user to determine when each instruction retires.
- Conventional trace encoding algorithms express what was executed, but not when. Cycle accurate trace lets the decoder know not just what got executed, but also when.

Whole system solutions

Debug and tracing data within a system doesn't end with the capture of the data. In addition to a comprehensive range of analytic, message, and communicator modules, Tessent also provides the software to analyze and interpret the trace results. Our SystemInsight IDE provides everything you need to ensure that your design is fully debugged when you need it to be.

Using Embedded Analytics components, you can debug and trace any design from simple single-processor systems to highly complex superscalar multi-processor systems.

Should you still require additional assistance, a highly-trained network of support-engineers is on hand to help you.



Siemens Digital Industries Software
siemens.com/eda

Americas +1 314 264 8499
Europe +44 (0) 1276 413200
Asia-Pacific +852 2230 3333

UL-002507-DS-5 | 11/22