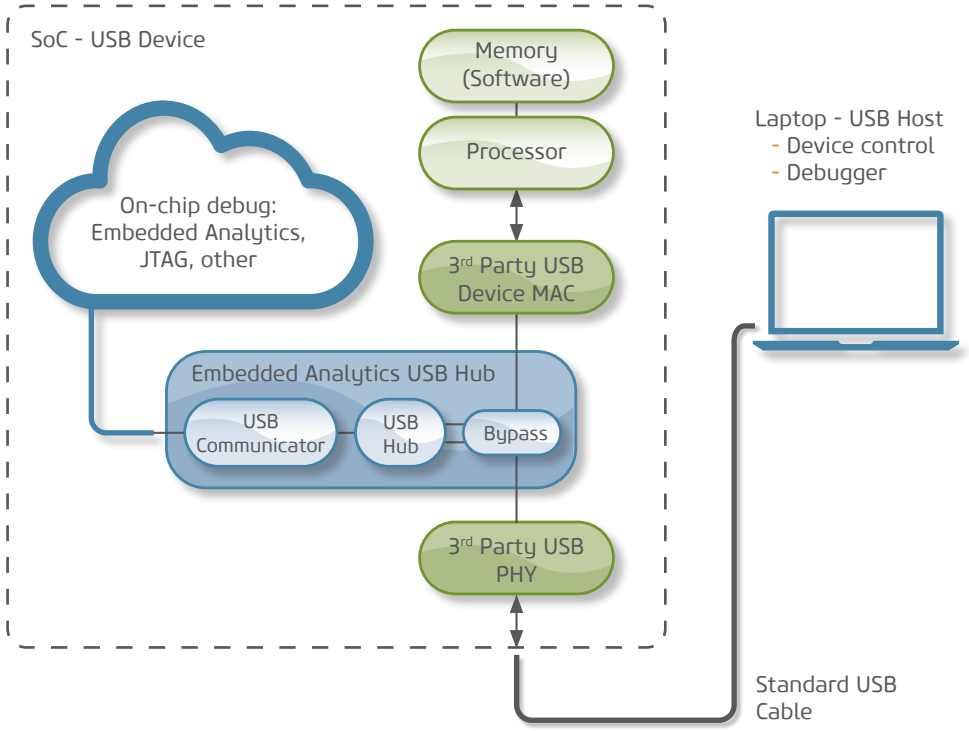
# ultraSoC USB Communicator

**The Tessent™ Embedded Analytics USB Communicator IP allows on-chip debug resources to connect to a PC using standard USB cable, sharing the chip's USB interface with system traffic and enabling high-speed debug access. The system is entirely hardware based ("bare metal"), requiring no processor or software stack, and so is completely non-intrusive and effective "from cycle zero" for bring-up.**




Any system debug architecture must access the outside world for configuration and to output data. Traditionally, designers have relied on debug-specific interfaces – typically JTAG – for this purpose.

The Tessent Embedded Analytics USB Communicator allows this to be done via an external interface – in this case USB – that is often already an intrinsic part of the device's design.

The approach brings many benefits. Dedicated debug I/O pins are not required, saving packaging costs. There is no need to purchase costly JTAG probes, and the USB 2.0 Communicator achieves at least 20x faster data rates than JTAG. Data rates of up to 10 Gbps are possible with the companion Embedded Analytics product, the EBC Communicator.

The interface is available "from cycle zero", allowing debug access before the main system OS has booted.

The Embedded Analytics USB Communicator is delivered as silicon IP for integration into any chip design. Together with the features of the Embedded Analytics Secure Message Infrastructure, access to the debug architecture can be controlled using authentication methods linked to the SoC security functions.

## At-a-glance

- USB 2.0
- Hardware-based: no CPU or stack
- Higher data rates via USB 3 companion product, (EBC Communicator)
- Fully compatible with on-chip debug fabrics: Embedded Analytics, JTAG and others
- Concurrent functional and debug traffic
- Zero impact on power states / transitions
- Stream trace data (eg ETM, RISC-V)
- Silicon-proven

## Functional overview

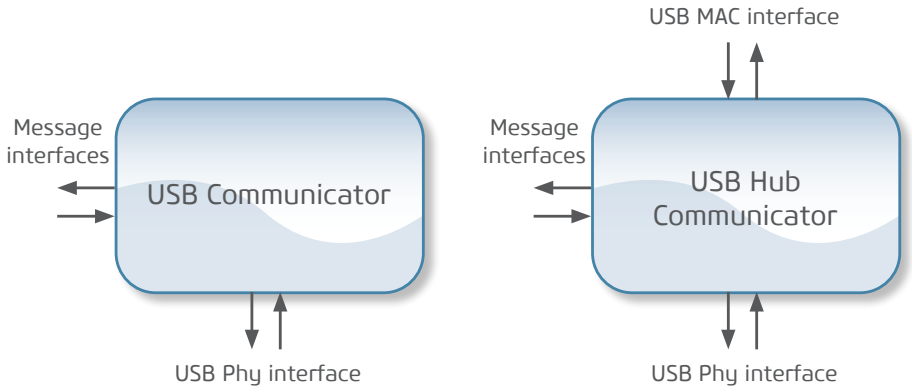
The USB Communicator provides high-speed debug communications from any debug host running common debug software (for example Lauterbach, GDB) to the Embedded Analytics system.

The USB 2.0 Communicator is delivered as Verilog RTL. The Communicator consists of a cut-down USB MAC that implements a fixed configuration for a pair of bulk data end-points. This is a hardware, state-machine based implementation of the standard USB protocol in “bare metal”. It is autonomous, requiring no host processor or software intervention. As such, it operates immediately from cycle zero and can be used to support debug immediately – even supporting bring-up and processor boot.

There are two variants of the USB Communicator. The first requires a dedicated USB PHY to be connected to it using either a ULPI or UTMI interface. The second includes a compound, two-port USB hub, allowing a single USB PHY to be connected and shared between the SoC’s functional requirements and the Embedded Analytics system.

A framing layer is implemented above the USB protocol which supports optional authentication.

A Windows driver is available.




The USB Communicator can be used for debug traffic only (left), or concurrent debug and system traffic (right)

### Product Features

- **Hardware-based USB controller**
  - No dependency on main system CPU / software
  - Delivered as parameterized soft core
- **USB 2.0: connect direct to debug host**
  - Debug probe not required
  - At least 20x faster than JTAG
- **Companion EBC Communicator provides USB 3.x SuperSpeed off-chip performance**
  - Requires EBC connection to SoC’s USB 3.x controller
- **Two Variants**
  - Direct connection for debug only
  - Integrated hub: debug and system traffic share single connection
- **Standard PHY interfaces (UTMI, UTMI+, ULPI)**