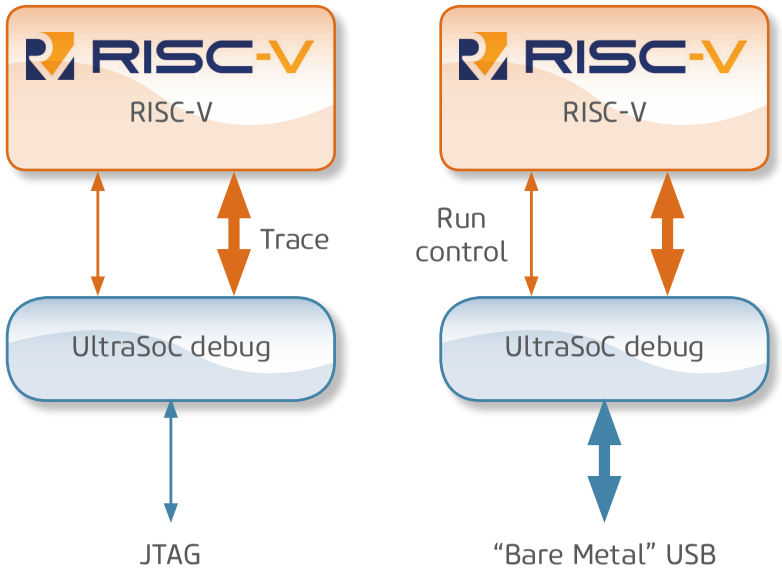
ultraSoC for RISC-V

UltraSoC offers a scalable debug and monitoring solution for developers using the RISC-V architecture. This can be a simple run control / JTAG system or support for full-speed processor trace. Designers can opt to choose from any elements within UltraSoC's SoC-wide solution for debug, performance monitoring and analytics, which supports monitoring of all major CPUs and custom logic, and protocol-aware probing of common buses.



RISC-V is a new open source instruction set architecture, initially developed by UC Berkeley but now being more widely adopted.

As a member of the RISC-V Foundation, UltraSoC is deeply involved in developing and defining the debug architecture for RISC V standards. UltraSoC fully supports both standards-based and proprietary debug approaches. We were the first company to offer a RISC-V processor trace solution, supporting both open source and commercial processors including those from Andes, Codasip, Microsemi, Roa Logic, SiFive and Syntacore.

We are also helping to define, and will fully support, the emerging processor trace specification.

In many SoC solutions, customers use UltraSoC for its sophisticated system level solutions, giving rich information for complex devices with multiple cores. However, UltraSoC's architecture is equally applicable for simpler devices, such as cost-sensitive uni-processor IoT systems. In these applications UltraSoC can simply implement standards compliant run-control and JTAG, together with a fully supported IDE.

At-a-glance

- Run control: halt, run, single step, break point
- Processor trace
- JTAG and cJTAG
- "Bare metal" USB
- Other connectivity options
- Standards compliant
- IDE support: Eclipse / GDB, TRACE32 and other solutions
- Non-intrusive, wire-speed
- Reduces post-silicon bring-up and debug burden

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The UltraSoC architecture

The UltraSoC architecture is designed from the ground up to provide a holistic, system-level view of the complex behaviors within today's SoCs, helping engineers develop and optimize SoC hardware and software in the lab and in-field.

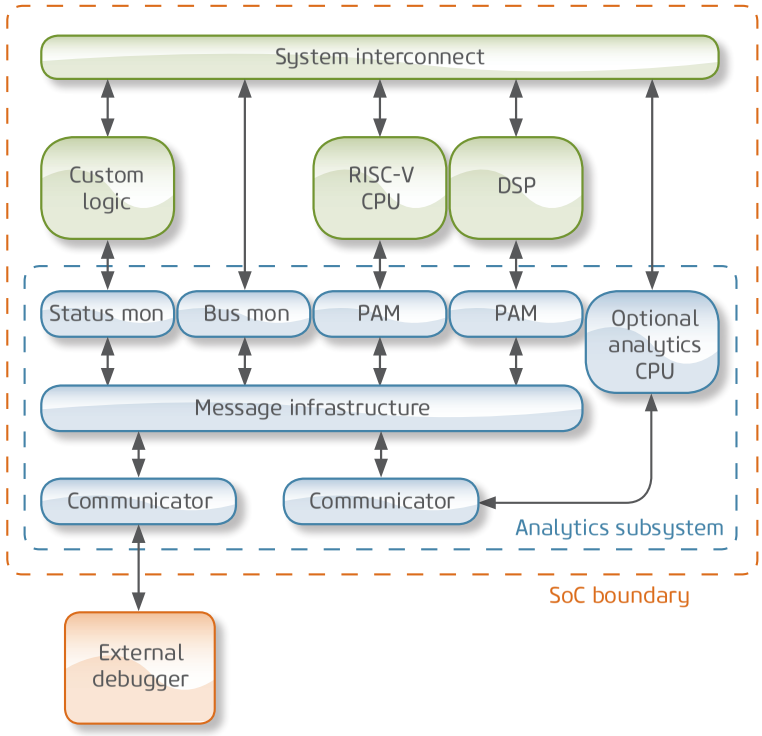
We offer a range of options for designers and architects working on RISC-V systems, ranging from simple run control and interconnect - with IDE support - to a full on-chip debug infrastructure. Our monitoring IP is designed to work with any processor, custom logic or bus protocol, making it particularly adept at dealing with heterogeneous systems containing multiple different processors.

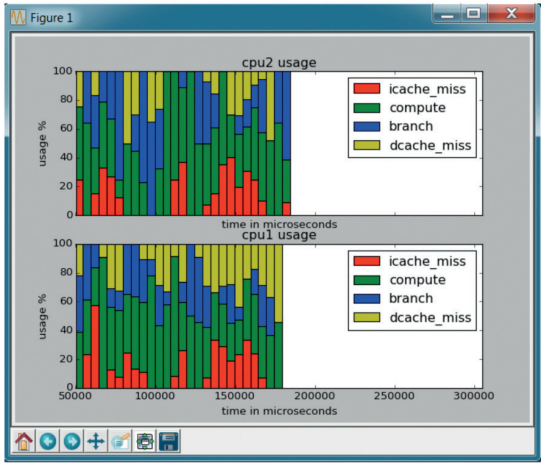
The modular, hierarchical UltraSoC architecture consists of three classes of IP block:

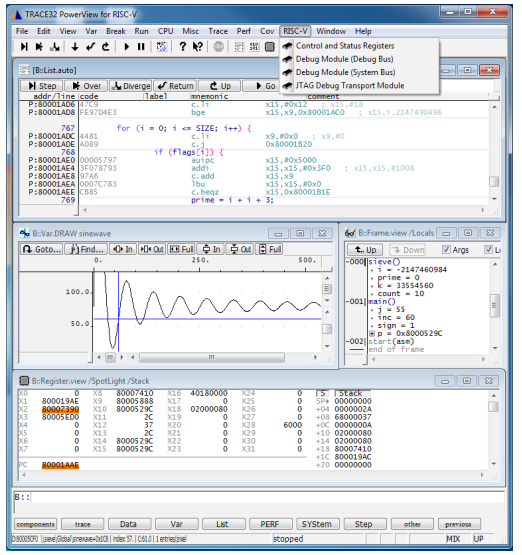
- Analytic modules: enable monitoring and control of system components
- Message infrastructure: dedicated fabric to connect UltraSoC components
- Communicators: interface the UltraSoC system to on-chip or external systems

By incorporating UltraSoC IP into a device, designers can intelligently monitor, understand and control the activity of any on-chip structure – including custom logic, buses, and CPU cores.

With low overhead of silicon area and power, and supported by partnerships with major development tool vendors, the UltraSoC architecture scales from low-cost embedded chips to the largest SoC project.







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